What is claimed is:

1. A digital duty cycle correction circuit comprising:

a clock rising edge generation means, which detects a rising edge of an input clock signal and generates a rising edge of a duty cycle corrected clock signal;

a clock falling edge generation means, which detects a rising edge of a clock signal that is 180° out of phase with the input clock signal and generates a falling edge of the duty cycle corrected clock signal based on the detected information; and

a clock delay means, which inverts a phase of the input clock signal by 180° and inputs the inverted input clock signal to the clock falling edge generation means .

2. The digital duty cycle correction circuit of claim 1, wherein the clock rising edge generation means and the clock falling edge generation means are included in a pseudo-C^2MOS-inverter.

3. The digital duty cycle correction circuit of claim 1, wherein the falling edge of the duty cycle corrected clock signal is generated according to the rising edge of the inverted input clock signal that is inverted by 180° by the clock delay means.

4. The digital duty cycle correction circuit of claim 1, further comprising a clock driving circuit means that outputs and provides the duty cycle corrected clock signal to external circuits and a digital duty cycle detection circuit means that detects the duty cycle corrected clock signal output from the clock driving circuit means and inputs the duty cycle corrected clock signal to the clock delay means.

5. The digital duty cycle correction circuit of claim 4, wherein the duty cycle detection circuit means controls the clock delay means and outputs a predetermined digital code that inverts the phase of the rising edge of the input clock signal by 180° and generates the rising edge of the duty cycle corrected clock signal.

6. The digital duty cycle correction circuit of claim 4, wherein the duty cycle detection circuit means comprises:

two integrators, which integrate a difference between a predetermined clock signal and a reference voltage over one period of the predetermined clock signal;

a comparator, which generates a predetermined down signal when an integrated value of the two integrators is greater than 0; and

a counter/register, which decreases or increases a count value by 1 according to the down signal or the up signal and stores predetermined information.

7. The digital duty cycle correction circuit of claim 6, wherein the predetermined information stored in the counter/register is in the form of a binary digital code of 4 bits.

8. The digital duty cycle correction circuit of claim 6, wherein the two integrators are equivalent.

9. A digital duty cycle correction method comprising:

(a) inverting a phase of an input clock signal by 180°;

(b) detecting a rising edge of the inverted clock signal; and

(c) generating a falling edge of a duty cycle corrected clock signal in response to the detected information,

wherein the falling edge of the duty cycle corrected clock is generated from the rising edge of the clock that is 180° out of phase with the input clock in step (a).